20% n-Type Silicon Solar Cell Fabricated by a Simple Process with an Aluminum Alloy Rear Junction and Extended Emitter

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***Abstract* — A simple process is defined and executed to achieve 20% efficiency for cells fabricated on 156 mm n-Cz Si wafers. The cell structure is n^+np^+ with the p^+ emitter being formed over most of the rear surface by Al alloying, but extended to the wafer edges by a light doping with B. The n^+ FSF is doped with P which makes the front surface easy to passivate and contact. B and P dopants are introduced into the wafer by ion implantation and are co-annealed in a single high temperature step, during which a passivating thermal oxide is also grown on the front and back surfaces. The back surface remains textured, and the entire process is additive as the cell structure is built layer-by-layer, with no subtractive steps needed for planarization, stripping diffusion glasses, or creating vias in dielectrics. A key benefit of the extended emitter is to improve p-n junction quality (since the depletion region is essentially confined within the interior of the silicon and does not intersect the surface), as indicated by the pseudo FF regularly exceeding 0.83. In addition, J_{sc} increases because of the reclaimed Si border area (Al to wafer edge). Cell parameters were found to be tightly distributed. The highest efficiency measured was 20.04% for a 239 cm^2 cell with a selective FSF and five busbars. Interconnecting cells in a module could be done with 3M Cu tape or Schmid Tin Pad applied directly to backside Al.**

***Index Terms* — silicon solar cells, n-type, Al alloy emitter, rear junction, ion implantation.**

I. INTRODUCTION

It is well known that monocrystalline n-type silicon wafers grown by the Czochralski method have certain advantages over similar p-type wafers for solar cells. Since n-type wafers have no boron doping, there is no light-induced degradation (LID) associated with the boron-oxygen defect. Furthermore, n-type wafers are more tolerant of metallic impurities present in a solar cell processing environment, such as iron, so that relatively high excess carrier lifetimes (> 1 ms) are fairly easy to achieve and maintain through the process – especially for high-resistivity wafers. However, processing n-type wafers into cells can be more complicated than processing their p-type counterparts. The Al BSF cell, which is fabricated from a p-type wafer and is the most common cell structure manufactured today, requires only a single phosphorus diffusion to form the front emitter. On the backside, aluminum is screen-printed and alloyed with silicon during the contact firing step. Exploiting the dual properties of aluminum as a contact metal and a p-type dopant enables the n^+pp^+ cell structure to be fabricated in a streamlined and cost-effective process. By adding a dielectric passivation layer to the back of the p-type wafer, a higher efficiency PERC structure results. Screen-printed aluminum still covers nearly the entire back of the cell, making contact to the p-type wafer only through vias in the dielectric. This combination of a phosphorus diffusion and screen-printed aluminum is a key reason that p-type Al BSF and PERC cells dominate the commercial solar cell world today, in spite of lower lifetimes, higher sensitivity to metallic impurities, and the LID associated with p-type wafers.

Attempts to take advantage of the superior material properties of n-type wafers, while retaining a conventional front junction cell structure, usually require two diffusions (front boron and back phosphorus) instead of one, and eliminates aluminum from the cell process. This adds complexity, since two high-temperature steps are now needed (with boron diffusion temperature typically about 100ºC above the phosphorus diffusion temperature) and with two silver printing steps needed (adding cost). Furthermore, making good electrical contact to a boron-doped emitter is somewhat challenging, with a Ag-Al paste usually required. In addition, the ease with which a phosphorus-doped emitted can be passivated is sacrificed when the front emitter is boron-doped.

Recently some researchers seeking to advance n-type cell technology have opted to continue using the easily-passivated and contacted n^+ surface on the front side of the cell and to continue using Al to contact a boron-doped emitter on the back side by making a rear junction n^+np^+ PERT (Passivated Emitter and Rear Totally diffused) structure [1, 2]. Since high excess carrier lifetimes in n-type wafers mean that minority carriers can be collected nearly equally well whether the p-n junction is at the front of the cell or at the rear, these approaches have yielded efficiencies significantly above 20%. However, these gains have come only with additional processing costs: the backside must be planarized, a p^+ rear emitter must be formed (e.g., by BBr_3 diffusion), a backside dielectric (e.g., Al_2O_3/SiN_x) must be deposited, and vias through the dielectric must be created prior to back aluminum

deposition. Note that multiple "subtractive" steps are required where material is removed, as in removing the backside Si texturing or backside texturing mask, stripping diffusion glasses, and removing the back dielectric in via formation.

There may be a middle ground, where the simple, additive, process of the Al BSF p-type cell is largely retained to produce an n-type cell having high efficiency. The purpose of this paper is to describe such a process and the 20% cells made by it.

II. Cell Structure and Process

The n-type analogue of the simple p-type Al BSF cell was first described in 2001 [3], where a 13.5%, 25 cm^2 cell fabricated on untextured, Sb-doped, thin (100 μm) dendritic web silicon was reported. This work showed that the quality, uniformity, and reproducibility of an Al alloy p-n junction is satisfactory for Si solar cells. Over time, the efficiency and area of such a rear junction cell increased to 18.5% [4]. In a contemporary study [5], an 18.6% Al alloy rear junction cell was fabricated on a 125 mm n-FZ substrate. As usual, this cell had a Si border around the edges, since Al cannot be screen-printed to the very edge of a wafer. This efficiency increased to 19.3% when 1 mm was trimmed from each of the wafer edges in an effort to extend the emitter to the very edge of the cell. After trimming, J_{sc} increased by 2.2%, FF increased by 1.0%, and V_{oc} increased by 0.3% to give a 3.5% (relative), or 0.7% (absolute), increase in efficiency. A similar 19.3% efficiency was obtained by [6] for an Al alloy rear junction cell fabricated from a 125 mm n-Cz wafer where the edges were trimmed by sawing as part of the edge isolation. Hence, it became clear that a significant increase in efficiency (0.7%) could be obtained by extending the rear emitter to the edge of the cell. However, physically removing material from the edge of the cell is not practical for production.

Rather, the rear emitter can be extended beyond the Al to the edge of the wafer by a separate B doping step, as shown in Fig. 1. Here, the front surface field (FSF) is shown as uniform. A selective FSF can also be employed. The process sequence for fabricating this cell is summarized in Table I.

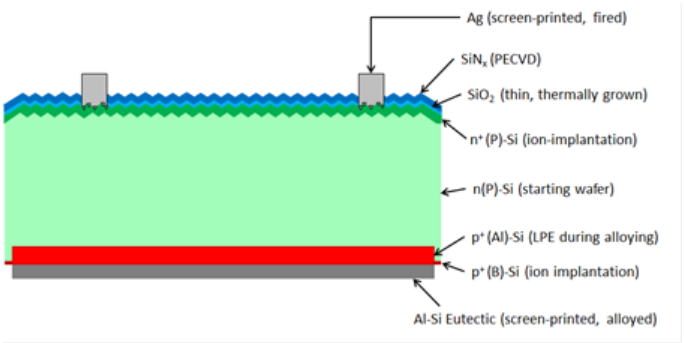

Fig. 1. Structure of Al alloy rear junction cell with extended emitter, as indicated by the short section labeled p^+(B).

TABLE I

Process Sequence for Fabricating Al Alloy Rear Junction Cell with Extended Emitter

1. Remove wafer saw damage and texture both sides
2. Implant B on back side (extended emitter)
3. Implant P on front side (FSF)
4. Co-anneal/oxidize (diffuse dopants, passivate surfaces)
5. Deposit SiN_x on front (AR coating)
6. Print/dry front Ag (front contact)
7. Print/dry back Al (back contact)
8. Co-fire Ag and Al (create main p-n junction)

Note that the process is quite simple, with just eight major steps. Both sides of the wafer are textured, and the back is not planarized. Furthermore, after texturing all steps are additive as the cell structure is built layer-by-layer. No subtractive steps where material is removed, such as diffusion glass, etch masks, or vias through a dielectric, are present. This makes for a streamlined, high-yield process flow.

The B dose is not critical, and can range from 1E14 to 2E15 B/cm^2 with implant energies ranging from 5 to 30 keV. A light B dose is preferred because of higher throughput and greater ease in passivating the doped surface. The P dose is typically about 3.4E15 P/cm^2 at 10 keV. Only one high-temperature step is needed, as B and P are co-annealed in a temperature range of 900ºC to 950ºC with O_2 flowing for 10 – 30 minutes. Total time from wafer load to wafer unload is approximately one hour. If desired, a selective FSF can be obtained by implanting a higher P dose beneath the front Ag contacts and a lower P dose between contacts. Note that implanted B supplements Al in creating the p^+ emitter over the Al area. Preferred n-wafer resistivity is 10 – 100 Ω-cm.

III. Cell Results

Cell results are summarized in Table II for in-house measurements made at Suniva and referenced to a cell calibrated by Fraunhofer CalLab. Cell parameters had a tight distribution, as indicated by the low standard deviations. The selective FSF provided an efficiency benefit of 0.26% (absolute) relative to uniform FSF cells. Best efficiency was 20.04%, with five of the 16 selective FSF cells reaching 20%.

TABLE II

Cell Results (n-Cz, 239 cm^2)

A. Uniform FSF (19 cells)

	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eff (%)
Average	38.19 ± 0.08	646.5 ± 0.3	79.64 ± 0.08	19.66 ± 0.05
Best	38.32	646.7	79.78	19.77

B. Selective FSF (16 cells)

	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eff (%)
Average	38.37 ± 0.11	649.1 ± 0.5	80.01 ± 0.10	19.92 ± 0.06
Best	38.51	649.4	80.12	20.04

Sheet resistance for the n^+ layer in the uniform FSF case was 80 Ω/□ and for the selective FSF was 98 Ω/□ between the front contacts and 72 Ω/□ beneath the contacts. The cells have five busbars on the front and no Ag on the back, as shown in Fig. 2.

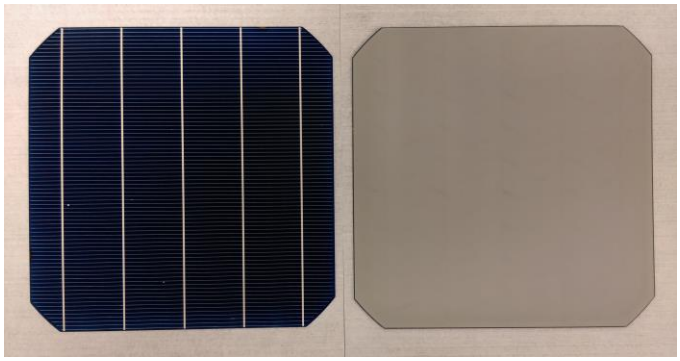

Fig. 2. Photograph of the front and back of an Al alloy rear junction cell with extended emitter (156 mm pseudosquare), fabricated according to the process of Table I.

Internal Quantum Efficiency and Reflectivity measurements were made at Suniva on the best selective FSF cell (10n5-16) and are shown in Fig. 3. The measurements indicate very good excess carrier lifetime in the bulk region (approximately 100% IQE from 550 nm to 970 nm), as required for a rear junction cell, and effective front surface passivation (92% IQE at 400 nm).

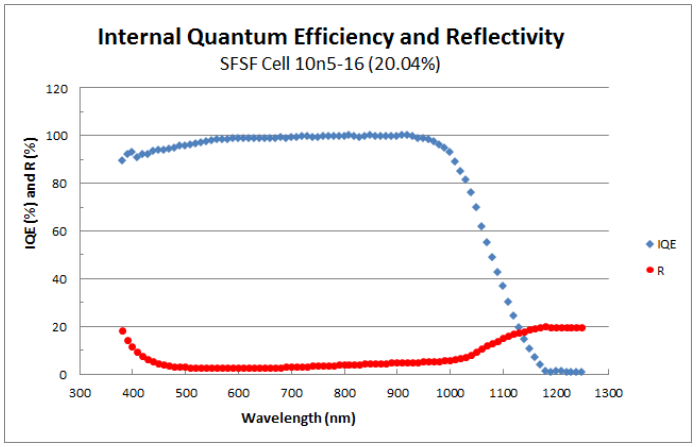

Fig. 3. Reflectivity and IQE data for cell 10n5-16 (20.04%).

Relative to the 18.5% FSF cell of [4], the best cell produced in this study (20.0%) has an efficiency 1.5% (absolute) higher. Of this difference, 0.7% is attributed to the extended B-doped emitter, as discussed earlier. An additional 0.4% is attributed to an increase from three busbars to five [7]. The remaining 0.4% is likely due to an improved co-anneal/oxidation process and to an improved front contact system with narrower grid lines contacting a higher sheet resistance FSF.

These cells with extended emitter had very good junctions, with ideality factors only slightly greater than unity (1.03) and high shunt resistance (24 kΩ-cm^2). Very good pseudo FF values (0.836) follow. This benefit is attributed to reduced recombination in the p-n junction depletion region, since the extended emitter forces the depletion region to remain almost entirely within the wafer and not intersect the back surface where surface recombination can occur. The result is a better quality junction with ideality factor close to unity and a high pseudo FF. With a typical series resistance for selective FSF cells of 0.717 Ω-cm^2, the resultant cell FF slightly exceeds 0.800.

There still remains the question of interconnecting such cells in a module by conventional soldering, since the back surface of the cell is fired Al which is not solderable. This problem can be solved by contacting the Al surface with a solderable material. Two successful approaches are Cu busbar tape by 3M [8] and Tin Pad by Schmid [9]. Both have been proven for full-sized modules using cells with full Al backs, and have met the IEC 61215 requirements for environmental testing.

IV. Possible Benefit of Segmenting Back Aluminum

It is worth considering dividing the back Al region into segments in order to increase cell efficiency while also reducing both the amount of Al paste required and the tendency of the cell to bow. Efficiency will increase if less recombination is associated with that part of the backside not covered by Al than with that part covered by Al.

The total J_0 for a cell is given by:

$$J_0 = J_{sc} * \exp(-V_{oc}/V_T) \qquad (1)$$

where V_T, the thermal voltage (kT/q) is 25.7 mV at 25ºC. Using J_{sc} (38.51 mA/cm^2) and V_{oc} (649.4 mV) from the best selective FSF cell of Table II, J_0 is calculated to be 409 fA/cm^2. This total J_0 is the sum of three components:

$$J_0 = J_{0n+} + J_{0n} + J_{0p+} \qquad (2)$$

where J_{0n+} is the component associated with recombination within the n^+ FSF region and its front Si surface, J_{0n} is the component associated with recombination within the bulk Si, and J_{0p+} is the component associated with recombination within the p^+ emitter region and its back Si surface (normally contacted by Al).

J_{0p+} needs to be determined from Eq. 2 for current cells as a benchmark which must be beaten for cell efficiency to increase. Values of J_{0n+} and J_{0n} can be estimated from symmetric test structures meant to mimic the n^+ and n regions of the current cells. Toward this end, symmetric n^+nn^+ test structures were created by implanting 2.6E15 P/cm^2 on each side of a lightly-doped n-Cz wafer and annealing the wafer at 900ºC for one hour in flowing O_2. This gives an n^+ sheet resistance of

80 Ω/□. After depositing PECVD SiN_x on both sides and sending the test structure wafers through a simulated contact firing (without metal) in a belt furnace, the structure $SiN_x/SiO_2/n^+nn^+/SiO_2/SiN_x$ was obtained. Photoconductivity decay measurements were then made to extract J_{0n+} (unmetallized) and high-level-injection lifetime (τ_{HLI}), according to [10]. Resultant values were J_{0n+} of 61 fA/cm^2 and τ_{HLI} of 1.93 ms. This value of τ_{HLI} translates to a J_{0n} value of 8 fA/cm^2 according to [4]. Front metal recombination losses are estimated at ~ 60 fA/cm^2 on an area-weighted (6% metal coverage) basis (~ 1000 fA/cm^2 full area) [11, 12]. With the calculated value of J_0 (409 fA/cm^2), along with estimated values of unmetallized J_{0n+} (57 fA/cm^2 for 94% of area), metallized J_{0n+} (60 fA/cm^2 for 6% of area) and J_{0n} (8 fA/cm^2), the value of J_{0p+} can be calculated from Eq. 2 to be 284 fA/cm^2. This represents the value appropriate for that part of the backside covered with alloyed Al.

One possible configuration for a segmented Al back is shown in Fig. 4, where the Al sheet is divided into a series of gridlines feeding into the back busbars. The back regions between the Al gridlines have been implanted with boron in Step 2 of Table I. This B dose, required to extend the emitter to the edges of the wafer, can be quite light so that the surface is well-passivated during the anneal/oxidation step (Step 4 of Table I). In this spirit, J_{0p+} for the back region not covered with Al is taken to be 70 fA/cm^2.

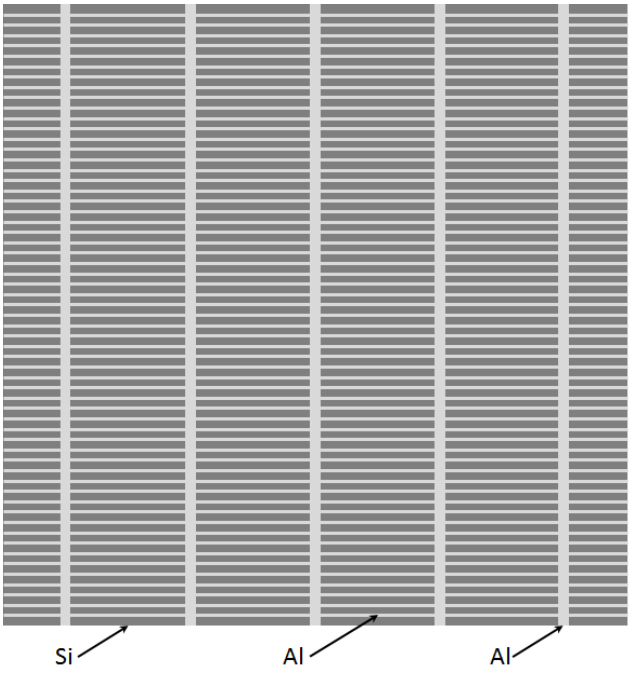

Fig. 4. Possible segmented Al pattern (gridlines feeding busbars).

With J_{0p+}(Al) of 284 fA/cm^2 and J_{0p+}(B) of 70 fA/cm^2, it is possible to compute an area-weighted average of J_{0p+} for any fraction of the back covered with Al. This weighted average of J_{0p+} can then be combined with J_{0n+} and J_{0n} to estimate total J_0 from Eq. 2. An estimated V_{oc} then follows from Eq. 1 assuming the J_{sc} value observed for the best selective FSF cell (38.51 mA/cm^2). Results are summarized in Table III.

The 25% back Al coverage could be obtained, for example, with Al gridlines that are 1 mm wide and having 3 mm space between these gridlines. Screen-printed and fired Al is sufficiently conductive (10 mΩ/□) that such 1 mm wide lines would add only marginal series resistance (0.024 Ω-cm^2) to a five-busbar cell, thereby decreasing efficiency by just 0.03% (absolute) relative to full Al coverage.

TABLE III

ESTIMATED V_{OC} AND EFFICIENCY AS AL FRACTION IS REDUCED

Back Al (%)	J_{0p+} (fA/cm^2)	J_0 (fA/cm^2)	V_{oc} (mV)	Eff (%)
100	284	409	649.4	20.04
75	230	355	653.0	20.15
50	177	3.2	657.2	20.28
25	124	249	662.1	20.43

In addition to the benefit of reduced J_{0p+} as back Al coverage is reduced, it is also expected that J_{sc} will increase for cells encapsulated in a module. This follows from light passing out of the cell between Al gridlines and being reflected from the white module backsheet back into the cell. With improved V_{oc} and J_{sc} resulting from reduced back Al coverage, it is conceivable that cell efficiency could reach 21% even as cost is reduced by using less Al paste.

V. SUMMARY

A cost-effective process for fabricating rear-junction n-type cells with efficiency slightly exceeding 20% was described. The process is based on ion implantation of phosphorus on the front side of the wafer and boron on the back side. A single high temperature step in the range of 900ºC - 950ºC with oxygen flowing is required to anneal implant damage, diffuse phosphorus and boron to their desired depths, and grow a passivating oxide on the front and back silicon surfaces. The total time from loading wafers into the oxidation furnace to unloading them is approximately one hour. From this point on, the usual processes required to produce Al BSF cells are executed, including deposition of PECVD SiN_x on the front, printing and drying the front Ag, printing and drying the back Al, and co-firing front and back contacts. The purpose of the backside boron is to extend the rear emitter formed by alloying Al to the edges of the wafer. The backside boron has multiple benefits: (1) it significantly reduces exposure of the p-n junction depletion region to the back silicon surface, thereby reducing recombination in the depletion region to increase FF and V_{oc} and (2) it extends the emitter to the edge of the wafer, thereby increasing J_{sc}. The amount of boron doping in this p^+ region is not critical, as a very light boron dose (high sheet resistance) is effective and this lightly-doped surface is easy to

passivate. Both sides of the wafer can remain textured, and after the saw damage is removed from the wafer at the beginning of the process all remaining steps are additive (no back planarization, stripping of diffusion glasses, or laser-drilling of vias). With a selective front surface field and a five busbar front contact, cell efficiencies up to 20.04% have been achieved. Interconnecting cells in a module could be done with the aid of either 3M backside busbar Cu tape or Schmid Tin Pad applied to the back aluminum surface to create a solderable surface. Finally, it may be possible to both reduce cost and increase efficiency (perhaps to 21%) by segmenting the back Al. A promising pattern is one of Al gridlines feeding into back Al busbars.

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